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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/483,570	01/14/2000	Gary L. Swoboda	TI-28933	8552

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2128	13

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Dm

Office Action Summary	Application N .	Applicant(s)	
	09/483,570	Swoboda	
	Examin r	Art Unit	
	Thai Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's brief filed on 01/02/2004. In view of the brief filed on 01/02/2004, the finality rejection on Aug. 01, 2003 is withdrawn. The rejection is set forth below.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al., US patent no. 6.075,941, in view of Key et al., US patent no. 6,173,386 B1.

As per claim 1, Itoh discloses a method of emulation of an integrated circuit including a CPU capable of executing program instruction with feature limitations substantially similar to the claimed invention (Abstract and Summary of the Invention). According to Itoh, the method includes steps of

detecting a predetermined debug event (col. 11, line 57 to col. 12, line 33, for example),

upon detection of the predetermined debug event suspending program execution except for at least one type of interrupt (col. 16, line 23 to col. 18, line 23),

and executing the monitor program during program debugged via at least one type interrupt (cols. 17-19).

Itoh further discloses the emulator (ICE) (14) having control function for monitoring and controlling the operation of the CPU processor via debug interrupt (Summary and Background of the Invention). Even Itoh does not expressly disclose an emulation monitor program, practitioner in the art at the time of the invention was made would have found Itoh ICE emulator program for monitoring and controlling the CPU processor operation as above could obviously imply emulation monitor program as claimed because the monitor program is executed and controlled in the emulator and for the emulator to monitor the operative state of the microcomputer.

Itoh does not expressly disclose selectively assigning control of at least emulation resource of the integrated circuit to one of the serial scan path or the emulation program as claimed. Such feature is however well known in the art. In fact, Key teaches a method and system for debugging a multiprocessor system (col. 4, lines 62-67 and col. 5, Summary of the Invention). The processor debugger selectively assigns control of at least debugging resources of the integrated circuit for emulation into serial scan registers (col. 8, lines 1-12, col. 19, line 39 to col. 20, line 7) in time division multiplexing scheme to determine resource failure in the multiprocessor system and reduce debugging time for such system as taught in Key.

This would motivate practitioner in the art at the time of the invention was made to combine Key debugger with feature of assigning control debugging resources for emulation of the integrated circuit to one of the serial scan path into Itoh emulator in order to determine resource failure and reduce debugging time in the complex integrated circuit.

As per claim 3, Itoh discloses a monitor program for monitoring priority interrupt, which could include privilege input for monitor program, monitoring privilege interrupt input for the emulation program, and assigning resources for emulation program and path tracing circuit.

As per claim 4, Itoh discloses emulation resources and accessing to the emulation resources through read/write data register (Figs. 3-20, col. 8, lines 26-59, cols. 9-13, for example). Key also teaches debugging resource and accessing resources through read and write operations in various data registers (col. 15, line 34 to col. 20, line 50).

Response to Arguments

1. Applicant's arguments with respect to claims 1, 3, and 4 have been considered but are moot in view of the new ground(s) of rejection.

2. In response to applicant's argument that Sample does not disclose selectively assigning emulation resources to the integrated circuit emulator, the examiner agrees with. Such argued feature is however known in the art. In fact, Key teaches a method and system for debugging a multiprocessor parallel system (col. 4, lines 62-67 and col. 5, Summary of the Invention). The processor debugger selectively assigns control of at least emulation or debugging resources of the integrated circuit into serial scan registers (col. 8, lines 1-12, col. 19, line 39 to col. 20, line 7) in time division multiplexing scheme to determine resource failure in the multiprocessor system and reduce debugging time for such system as taught in Key.

This would motivate practitioner in the art at the time of the invention was made to combine Key debugger with feature of assigning control emulation resource of the integrated circuit to one of the serial scan path into Itoh emulator in order to determine resource failure and reduce debugging time in the complex integrated circuit.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 6,385,747 B1, issued to Scott et al., on May 2002
2. US patent no. 6,446,221 B1, issued to Jaggar et al., on Sept. 2002
3. US patent no. 6,681,341 B1, issued to Fredenburg et al., on Jan. 2004

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is 703-305-3812.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thai Phan
Feb. 25, 2004

Thaiphan
Thai Phan
Patent Examiner
AU: 2128